

**REMARKS**

Claims 1-2 and 5-16 are all the claims pending in the application.

Claims 1 and 10 has been amended to further clarify the claimed invention.

Claims 8 and 9 have been rewritten in independent form.

Claim 12 has been amended in response to the claim objections.

Applicants thank the Examiner for indicating that claims 1 and 14-16 contain allowable subject matter.

**CLAIM OBJECTIONS**

The Examiner objects to claim 12 as containing an informality. Claim 12 has been amended to address the objection. Therefore, the Examiner is requested to withdraw the objection.

**PRIOR ART REJECTIONS**

The Examiner has rejected claims 1, 5, 6, 8-10 and 13 under 35 U.S.C. § 102(e) as being anticipated by, or in the alternative, under 35 U.S.C. § 103(a) as obvious over Subraya (U.S. Patent App. No. 2007/0210433). Applicants traverse these rejections because Subraya is not prior art. Subraya has a U.S. filing date of March 8, 2006. However, the present application is based on, and claims priority to, provisional application No. 60/459,353, which was filed on April 2, 2003. The current claims are fully support in the provisional application. Therefore, the Examiner is requested to withdraw the rejections based on Subraya.

The Examiner has rejected claims 1, 5<sup>1</sup>, 7, 10 and 11 under 35 U.S.C. § 102(e) as being anticipated by, or in the alternative, under 35 U.S.C. § 103(a) as obvious over Lee (U.S. Patent

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<sup>1</sup> The Office Action does not list claim 5 as being rejected by Lee. However, Applicant's attorney contacted the Examiner, who confirmed that claim 5 should have been rejected.

No. 7,005,316). Applicants traverse these rejections because Lee fails to disclose or suggest all of the claim limitations. Specifically, Lee fails to disclose or suggest at least the following limitations:

wherein said secondary IC structure is mounted on said first chip face of said base IC structure.

One embodiment of the claimed invention is shown in Figure 5. Figure 5 shows that the two IC structures are oriented in the same direction, with the chip being on top of the substrates (based on the view of figure 5). Thus, the secondary IC structure 400 is mounted on the chip face 315a of the base IC structure.

On the other hand, the two IC structures in Lee are oriented in opposite directions. Thus, the two substrates are mounted to each other; rather than one substrate being mounted to the chip surface of the other IC structure, as required by claim 1, and similarly by claim 10.

In addition, Applicant respectfully disagrees that Lee discloses or suggests a first encapsulant providing a structure that enables mounting of said secondary IC structure on said base IC structure. In Lee, the two substrates are first attached via solder balls and then an encapsulant fills the open space.

Dependent claim 5, 7 and 11 should also be allowable, at least based on their dependence from claim 1 or 10.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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